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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,540	12/28/2005	Vasanth R. Gaddam	US030205	5888

24737 7590 08/19/2008

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
WYLLIE, CHRISTOPHER T	
ART UNIT	PAPER NUMBER
2619	
MAIL DATE	DELIVERY MODE
08/19/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,540	GADDAM ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER T. WYLLIE	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 1-22 are pending in Application 10/562,540.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Strolle et al. (US 2004/0028076).

Regarding claim 21, Strolle et al. discloses a data de-randomizer **(see Figure 3A, De-randomizer 334)** for use in a television receiver **(see Figure 3, Digital television Receiver 316)** capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream **(paragraph 0078, lines 2-8 [the enhanced signals is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet stream for the digital television receiver and a robust packet stream])**, said data de-randomizer comprising: a standard de-randomizer capable of de-randomizing bytes associated with said standard stream; and a robust de-randomizer capable of de-randomizing bytes associated with said robust stream

(paragraph 0084, lines 12-14 [the VSB De-randomizer is operates on both the normal and robust bytes]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 7-8, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. (US 2004/0028076) in view of Limberg (2004/0237024).

Regarding claim 1, Strolle et al. discloses a packet formatter **(see Figure 3, Demodulator/Decoder 314)** for use in a television receiver capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream **(paragraph 0078, lines 2-8 [the enhanced signals is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet stream for the digital television receiver and a robust packet stream])**, said packet formatter comprising: a first processing block (410) capable of receiving said dual bitstream signal and removing therefrom header bits and parity bits associated with said robust stream to thereby produce a first output signal **(paragraph 0084, lines 7-9 and paragraph 0085, lines 5-7 [the Reed-Solomon decoder of the Demodulator/Decoder strips parity bytes off the robust packet stream and only information bytes are sent to the de-randomizer; the first three byte header for every 187 robust byte packet is removed])**. Strolle et al. does not disclose a second processing block capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter. However, Limberg discloses such a feature **(paragraph 0204, lines 15-17 [the output from the Decoder 113 is the input to the 2:1 Compressor 111 which deletes all redundant alternate bits from the payload])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Limberg into the system of Strolle et al. The method of Limberg can be implemented by incorporating a 2:1 Compressor into the television receiver. The motivation for this is to remove error correction (redundant bits) performed by the Forward Error Correction (FEC) Coders.

Regarding claim 7, Strolle et al. does not disclose a signal comprising the second output signal from the data path of the packet formatter. However, Limber further discloses such a feature **(see Figure 22B, 2:1 Compressor 114 and Data De-randomizer 115 [after the 2:1 Compressor deletes the redundant bits, that data is sent to the Data De-randomizer])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Limberg into the system of Strolle et al. The method of Limberg can be implemented by enabling the 2:1 Compressor to forward the filtered signal to the De-randomizer. The motivation for this is to provide a signal to the De-randomizer without redundant robust bits in order to produce a steady stream of robust data and normal data.

Regarding claim 8, Strolle et al. discloses a television receiver (200) capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream **(paragraph 0078, lines 2-8 [the enhanced signals is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet stream for the digital television receiver and a robust packet stream])**, a method of

formatting packets of said dual bitstream signal comprising the steps of: receiving in a packet formatter (240) said dual bitstream signal and removing therefrom header bits and parity bits associated with said robust stream to thereby produce a first output signal**(paragraph 0084, lines 7-9 and paragraph 0085, lines 5-7 [the Reed-Solomon decoder of the Demodulator/Decoder strips parity bytes off the robust packet stream and only information bytes are sent to the de-randomizer; the first three byte header for every 187 robust byte packet is removed])**. Strolle et al. does not disclose receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter. However, Limberg discloses such a feature **(paragraph 0204, lines 15-17 [the output from the Decoder 113 is the input to the 2:1 Compressor 111 which deletes all redundant alternate bits from the payload])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Limberg into the system of Strolle et al. The method of Limberg can be implemented by incorporating a 2:1 Compressor into the television receiver. The motivation for this is to remove error correction (redundant bits) performed by the Forward Error Correction (FEC) Coders.

Regarding claim 14, Strolle et al. does not disclose a signal comprising the second output signal from the data path of the packet formatter. However, Limber further discloses such a feature **(see Figure 22B, 2:1 Compressor 114 and Data De-**

randomizer 115 [after the 2:1 Compressor deletes the redundant bits, that data is sent to the Data De-randomizer]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Limberg into the system of Strolle et al. The method of Limberg can be implemented by enabling the 2:1 Compressor to forward the filtered signal to the De-randomizer. The motivation for this is to provide a signal to the De-randomizer without redundant robust bits in order to produce a steady stream of robust data and normal data.

Regarding claim 15, Strolle et al. discloses a television receiver **(see Figure 3, Digital Television Receiver 316)** comprising: receiver front-end circuitry **(see Figure 3, Demodulator/Decoder 314)** capable of receiving and down-converting a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream to thereby produce a baseband signal **(paragraph 0078, lines 2-8 [the enhanced signals is received by the Demodulator/Decoder 314 and separates the signal to produce a normal packet stream for the digital television receiver and a robust packet stream])**; and a first processing block (410) capable of receiving said standard stream and said robust stream associated with said baseband signal and removing therefrom header bits and parity bits associated with said robust stream to thereby produce a first output signal **(paragraph 0084, lines 7-9 and paragraph 0085, lines 5-7 [the Reed-Solomon decoder of the Demodulator/Decoder strips parity bytes off the robust packet stream and only information bytes are sent to the de-randomizer; the first three**

byte header for every 187 robust byte packet is removed]). Strolle et al. does not disclose a forward error correction section capable of receiving said baseband signal from said receiver front-end circuitry wherein said forward error correction section comprises a packet formatter and a second processing block capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output of said packet formatter. However, Limberg discloses such a feature **(see Figure 22B R-S FEC Decoder 113 and paragraph 0204, lines 15-17 [the R-S FEC Decoder processes the signal; the output from the R-S FEC Decoder 113 is the input to the 2:1 Compressor 111 which deletes all redundant alternate bits from the payload])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Limberg into the system of Strolle et al. The method of Limberg can be implemented by incorporating an R-S FEC decoder and a 2:1 Compressor into the television receiver. The motivation for this is to remove error correction (redundant bits) performed by the Forward Error Correction (FEC) Coders.

8. Claims 2, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. (US 2004/0028076) in view of Limberg (2004/0237024) as applied to claim 1 and 8 above, and further in view of Hurst, Jr. (US 6,034,731).

Regarding claim 2, the references as applied above disclose all the claimed subject matter recited in claim 1, but do not disclose that the packet formatter passes

bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time. However, Hurst, Jr. discloses such a feature **(column 4, lines 2-5 [the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Hurst, Jr. into the system of the references as applied above. The method of Hurst, Jr. can be implemented by enabling the Demodulator/Decoder 314 to determine the amount of time to wait to decode the picture. The motivation for this is to synchronize the audio and video output on to the television receiver.

Regarding claim 9, the references as applied above disclose all the claimed subject matter recited in claim 8, but do not disclose that the packet formatter passes bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time. However, Hurst, Jr. discloses such a feature **(column 4, lines 2-5 [the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Hurst, Jr. into the system of the references as applied above. The method of Hurst, Jr. can be implemented by enabling the Demodulator/Decoder 314 to determine the amount of time to wait to

decode the picture. The motivation for this is to synchronize the audio and video output on to the television receiver.

Regarding claim 16, the references as applied above disclose all the claimed subject matter recited in claim 15, but do not disclose that the packet formatter passes bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time. However, Hurst, Jr. discloses such a feature **(column 4, lines 2-5 [the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Hurst, Jr. into the system of the references as applied above. The method of Hurst, Jr. can be implemented by enabling the Demodulator/Decoder 314 to determine the amount of time to wait to decode the picture. The motivation for this is to synchronize the audio and video output on to the television receiver.

9. Claims 3-6, 10-13, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. (US 2004/0028076) in view of Limberg (2004/0237024) in view of Hurst, Jr. (US 6,034,731) as applied to claim 2 above, and further in view of Fimoff (US 2001/0055342).

Regarding claim 3, the references as applied above disclose all the claimed subject matter recited in claim 2, but do not disclose a third processing block capable of

determining the locations of the parity bits in the robust stream. However, Fimoff discloses such a feature **(paragraph 0053, lines 4-12 and see Figure 9, Robust VSB Receiver 130, Discard Block 136, and Discard Line 134 [the discard block discards transport headers and parity symbols within the robust VSB data at locations indicated by the discard line 134])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the Robust Post Processor 340 (Strolle et al.) to discard headers and parity symbols at known locations within the robust stream. The motivation for this is to send relevant portions of the robust stream to the receiver.

Regarding claim 4, the references as applied above do not disclose that the third processing block is capable of determining the locations of the header bits in the robust stream. However, Fimoff discloses such a feature **(paragraph 0053, lines 4-12 and see Figure 9, Robust VSB Receiver 130, Discard Block 136, and Discard Line 134 [the discard block discards transport headers and parity symbols within the robust VSB data at locations indicated by the discard line 134])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the Robust Post Processor 340 (Strolle et al.) to discard headers and parity symbols at

known locations within the robust stream. The motivation for this is to send relevant portions of the robust stream to the receiver.

Regarding claim 5, Strolle et al further discloses that the third processing block contains a look-up table (paragraph 0079, lines 10-16 **[a complete map of VSB symbols indicating whether each symbol is robust or normal is assembled in block 323])**.

Regarding claim 6, the references as applied above do not disclose that the packet formatter generates and outputs packet identification used by subsequent processing blocks. However, Fimoff further discloses such a feature **(paragraph 0043, lines 1-7 [the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the packet formatter to decode the PID's from the data stream. The motivation for this is to determine which packets will be forwarded to the RVSB receiver based on the PID.

Regarding claim 10, the references as applied above disclose all the claimed subject matter recited in claim 9, but do not disclose a third processing block capable of determining the locations of the parity bits in the robust stream. However, Fimoff discloses such a feature **(paragraph 0053, lines 4-12 and see Figure 9, Robust VSB**

Receiver 130, Discard Block 136, and Discard Line 134 [the discard block discards transport headers and parity symbols within the robust VSB data at locations indicated by the discard line 134]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the Robust Post Processor 340 (Strolle et al.) to discard headers and parity symbols at known locations within the robust stream. The motivation for this is to send relevant portions of the robust stream to the receiver.

Regarding claim 11, the references as applied above do not disclose that the third processing block is capable of determining the locations of the header bits in the robust stream. However, Fimoff discloses such a feature **(paragraph 0053, lines 4-12 and see Figure 9, Robust VSB Receiver 130, Discard Block 136, and Discard Line 134 [the discard block discards transport headers and parity symbols within the robust VSB data at locations indicated by the discard line 134])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the Robust Post Processor 340 (Strolle et al.) to discard headers and parity symbols at known locations within the robust stream. The motivation for this is to send relevant portions of the robust stream to the receiver.

Regarding claim 12, Strolle et al further discloses that the third processing block contains a look-up table (paragraph 0079, lines 10-16 **[a complete map of VSB symbols indicating whether each symbol is robust or normal is assembled in block 323])**.

Regarding claim 13, the references as applied above do not disclose that the packet formatter generates and outputs packet identification used by subsequent processing blocks. However, Fimoff further discloses such a feature **(paragraph 0043, lines 1-7 [the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the packet formatter to decode the PID's from the data stream. The motivation for this is to determine which packets will be forwarded to the RVSB receiver based on the PID.

Regarding claim 17, the references as applied above disclose all the claimed subject matter recited in claim 16, but do not disclose a third processing block capable of determining the locations of the parity bits in the robust stream. However, Fimoff discloses such a feature **(paragraph 0053, lines 4-12 and see Figure 9, Robust VSB Receiver 130, Discard Block 136, and Discard Line 134 [the discard block**

discards transport headers and parity symbols within the robust VSB data at locations indicated by the discard line 134]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the Robust Post Processor 340 (Strolle et al.) to discard headers and parity symbols at known locations within the robust stream. The motivation for this is to send relevant portions of the robust stream to the receiver.

Regarding claim 18, the references as applied above do not disclose that the third processing block is capable of determining the locations of the header bits in the robust stream. However, Fimoff discloses such a feature **(paragraph 0053, lines 4-12 and see Figure 9, Robust VSB Receiver 130, Discard Block 136, and Discard Line 134 [the discard block discards transport headers and parity symbols within the robust VSB data at locations indicated by the discard line 134])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the Robust Post Processor 340 (Strolle et al.) to discard headers and parity symbols at known locations within the robust stream. The motivation for this is to send relevant portions of the robust stream to the receiver.

Regarding claim 19, Strolle et al further discloses that the third processing block contains a look-up table (paragraph 0079, lines 10-16 **[a complete map of VSB**

symbols indicating whether each symbol is robust or normal is assembled in block 323]).

Regarding claim 20, the references as applied above do not disclose that the packet formatter generates and outputs packet identification used by subsequent processing blocks. However, Fimoff further discloses such a feature **(paragraph 0043, lines 1-7 [the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of Fimoff into the system of the references as applied above. The method of Fimoff can be implemented by enabling the packet formatter to decode the PID's from the data stream. The motivation for this is to determine which packets will be forwarded to the RVSB receiver based on the PID.

Conclusion

10. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER T. WYLLIE whose telephone number is (571) 270-3937. The examiner can normally be reached on Monday through Friday 8:30am to 6:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher T. Wyllie/
Examiner, Art Unit 2619

/Edan Orgad/
Supervisory Patent Examiner, Art Unit 2619